Notice of Allowability	Application No. 10/026,679	Applicant(s) ACHLER, ISAAC	
	Examiner Salman Ahmed	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/17/2001*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No._____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-8 are allowed.

2. The following is an examiner's statement of reasons for allowance: The instant application claims a data optimization engine for optimizing selected frames of a first stream of data, comprising- a transmit interface circuit coupled to an optimization processor, transmit interface circuit being configured for receiving first stream of data, transmit interface circuit includes a traffic controller circuit for separating frames in first stream of data into a first optimizable frame and a first non-optimizable frame, and an optimization front-end circuit coupled to traffic controller circuit to receive at least a first portion of first optimizable frame, optimization front-end circuit including a protocol conversion circuit configured to convert data in first portion of first optimizable frame from a first protocol to a second protocol suitable for processing by optimization processor, first protocol specifies a first word length, second protocol specifies a second word length different from first word length, optimization front-end circuit further includes an end-of-optimization-tile processing circuit, end-of-optimization-file processing circuit flagging an end of first portion of first optimizable frame to optimization processor, wherein optimization processor is configured to optimize first portion of first optimizable frame by performing at least one of compression and encryption on first portion of first optimizable frame.

The cited prior art Witt (US PAT 6321326) teaches a microprocessor being configured to execute a prefetch instruction specifying a cache line to be transferred into

the microprocessor, as well as an access mode for the cache line. The microprocessor includes caches optimized for the access modes. In one embodiment, the microprocessor includes functional units configured to operate upon various data type. Each different type of functional unit may be connected to different caches, which are optimized for the various access modes. The prefetch instruction may include a functional unit specification in addition to the access mode. In this manner, data of a particular type may be prefetched into a cache local to a particular functional unit.

The cited prior art Devoe (US PAT PUB 2002/0165957) teaches a method for building a network route map is described in which network operational characteristics are gathered by actively probing multiple network routes, and building the network route map based on the operational characteristics. Route maps are generated which provide a view of the network from the perspective of a particular routing device in the network. Embodiments include methods for gathering the operational data by transmitting one or more data packets, receiving responses thereto, and determining time differentials based on the responses. Other embodiments include methods for processing the operational data to determine various metrics, and normalizing the data with similar data gathered from other network route probes. Finally, additional embodiments include propagation of the preferred route information to multiple routing devices to provide intelligent route select.

The cited prior art Holzle et al. (US PAT 6237141), hereinafter referred to as Holzle teaches methods and apparatus for dynamically determining whether portions of code should be interpreted or compiled in order to optimize a software application

during run-time are disclosed. According to one aspect of the present invention, computer-implemented method for run-time processing of a computer program, which includes byte-codes, arranged as a plurality of methods includes invoking a first method selected from the plurality of methods. Invoking the first selected method involves interpreting the first selected method. An invocation tracker, which is arranged to track the number of invocations of the first selected method, is updated, and a determination is made regarding when the invocation tracker indicates that the number of invocations of the first selected method exceeds a threshold value. The first selected method is compiled when it is determined that the invocation tracker indicates that the number of invocations of the first selected method exceeds a threshold value. This threshold value is periodically adjusted to keep the compilation and the interpretation overheads within acceptable ranges.

The cited prior art Holzle (US PAT 5933635) teaches methods and apparatus for dynamically deoptimizing a frame in a control stack during the execution of a computer program are disclosed. The described methods are particularly suitable for use in computer systems that are arranged to execute both interpreted and compiled byte codes. According to one aspect of the present invention, a computer-implemented method for deoptimizing a compiled method includes creating a data structure. The data structure, which is separate from the control stack, is arranged to store information relating to the compiled method. A reference indicator, such as a pointer, is created to associate the data structure with the frame. The method, which is compiled to a first state of optimization, is then deoptimized to a second state of optimization, and the

method in the first state of optimization may be discarded, thereby deoptimizing the frame. When control returns to the deoptimized frame, a migration routine creates at least one new stack frame, and execution may continue using the method in the second state of optimization.

An IEEE Oct. 1988 publication *Massively parallel data optimization* by Knobe et al., hereinafter referred to as Knobe, teaches techniques for the automatic layout of arrays in a Fortran compiler supporting Fortran 8× array features and targeted to the Connection Machine computer system. The goal is primarily to minimize the costs of moving data between processors and secondarily to minimize memory usage. Improved array layout may allow communications operations to be eliminated or to be replaced by more specialized communications operations with lower costs. The potential performance impact of this compilation technology is measured in orders of magnitude rather than percentages

The cited prior arts alone or in combination fail to jointly suggest or teach the claimed combination of features as taught by the instant application. Witt, Devoe, Holzle and Knobe do not specifically teach a data optimization engine for optimizing selected frames of a first stream of data, comprising- a transmit interface circuit coupled to an optimization processor, transmit interface circuit being configured for receiving first stream of data, transmit interface circuit includes a traffic controller circuit for separating frames in first stream of data into a first optimizable frame and a first non-optimizable frame, and an optimization front-end circuit coupled to traffic controller circuit to receive

at least a first portion of first optimizable frame, optimization front-end circuit including a protocol conversion circuit configured to convert data in first portion of first optimizable frame from a first protocol to a second protocol suitable for processing by optimization processor, first protocol specifies a first word length, second protocol specifies a second word length different from first word length, optimization front-end circuit further includes an end-of-optimization-tile processing circuit, end-of-optimization-file processing circuit flagging an end of first portion of first optimizable frame to optimization processor, wherein optimization processor is configured to optimize first portion of first optimizable frame by performing at least one of compression and encryption on first portion of first optimizable frame.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571)272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Salman Ahmed
Examiner
Art Unit 2666

SA